CLAIMS

1. An apparatus comprising:

a circuit comprising a distributed multiplexer configured to receive a distributed input group of signals, wherein said distributed multiplexer is configured to evenly load said distributed input groups.

2. The apparatus according to claim 1, wherein said distributed multiplexer comprise a plurality of bits each configured to evenly load said input groups.

3. The apparatus according to claim 2, wherein said bits of one distributed multiplexer are interleaved with at least another distributed multiplexer.

4. The apparatus according to claim 1, wherein said circuit comprises a programmable interconnect matrix (PIM).

5. The apparatus according to claim 3, wherein said bits comprise programmable interconnect matrix (PIM) bits.

6. The apparatus according to claim 1, wherein said circuit is configured to provide flexible reprogramming of said distributed multiplexer.

7. The apparatus according to claim 1, wherein said circuit is scalable.

8. The apparatus according to claim 7, wherein a configuration of said circuit is expandable in a horizontal direction.

9. The apparatus according to claim 8, wherein said configuration of said circuit is expandable in a vertical direction.

10. The apparatus according to claim 9, wherein said configuration reduces complexity of physical routes of said distributed input groups.

11. The apparatus according to claim 1, wherein a layout of said circuit is deterministic.

12. The apparatus according to claim 1, wherein a delay of said circuit is deterministic.

13. An apparatus comprising:

one or more input groups; and

one or more configurable matrices each configured to generate an output in response to said input groups, wherein said input groups are shared across said configurable matrices.

14. The apparatus according to claim 13, wherein said input groups are constant across said configurable matrices.

15. The apparatus according to claim 13, wherein each of said configurable matrices comprise:

one or more multiplexers configured to generate said output in response to said input groups.

16. The apparatus according to claim 15, wherein said multiplexers comprise:

two or more bits configured to generate said output in response to said input groups.

17. The apparatus according to claim 13, further comprising:

a plurality of input groups; and

a plurality of configurable matrices.

18. The apparatus according to claim 17, wherein said plurality of input groups are shared across said plurality of configurable matrices.

19. The apparatus according to claim 13, wherein said configurable matrices have a deterministic delay.

20. The apparatus according to claim 13, wherein a layout area of said apparatus is defined by said configurable matrices.